## REMARKS

### Claim Rejections – 35 U.S.C. §103(a)

The Examiner has rejected base Claim 1 under 35 U.S.C. 103(a) as being rendered obvious by art cited in Hanafi et al, Lin et al. and Sugishima et al. It is Applicant's understanding that Hanafi et al, Lin et al, and Sugishima et al neither teach nor render obvious the invention specified in claims 1-6 and claims 8-11.

Applicant claims in claims 1-6 a method of forming a replacement gate stack. The method comprises "forming a sacrificial gate electrode over a substrate and "forming **carbon-doped sidewall spacers without oxide components** on the sides of the sacrificial gate electrode. The method further comprises "forming a sacrificial inter-level dielectric layer comprising a **stoichiometric silicon nitride**, removing the sacrificial gate electrode, depositing a replacement gate electrode, polishing the sacrificial inter-level dielectric layer and the replacement gate electrode, and performing a wet etch removal on the sacrificial inter-level dielectric layer." That is, Applicant claims a method of forming a replacement gate stack which includes forming **carbon doped** sidewall spacers without oxide components and a sacrificial inter-level dielectric layer comprising a **stoichiometric silicon nitride**.

It is Applicant's understanding that Hanafi et al fails to disclose a method of forming a replacement gate stack which includes forming carbon doped sidewall spacers without oxide components and a sacrificial inter-level dielectric layer comprising a stoichiometric silicon nitride. Hanafi et al does disclose forming a sacrificial gate electrode (24) on a substrate (10), forming sidewall spacer (26) on the sides of the gate, and forming a sacrificial inter-level dielectric layer (28). Hanafi et al further discloses removing the sacrificial gate electrode, forming replacement gates, polishing the replacement gate and sacrificial dielectric, and removing the inter-level dielectric layer. Furthermore, it is Applicants' understanding that Hanafi et al discloses sidewall spacers comprising silicon nitride (column 4, line 38). Moreover, it is also Applicants' understanding that Hanafi et al discloses a sacrificial inter-level dielectric layer comprising a high-density plasma (HDP) oxide or tetra-ethyl ortho silicate (TEOS)

(column 4 lines 49-51). As such, it is Applicants' understanding that Hanafi et al does not render obvious forming a replacement gate stack which includes forming carbon doped sidewall spacers without oxide components and a sacrificial inter-level dielectric layer comprising a stoichiometric silicon nitride.

Additionally, it is Applicants' understanding that neither of the secondary references, Lin et al nor Sugishima et al, renders a method of forming a replacement gate stack which includes forming carbon doped sidewall spacers without oxide components and a sacrificial inter-level dielectric layer comprising a stoichiometric silicon nitride. Lin et al discloses CMP polishing the replacement gate and dielectric layer to planarize (column 5 lines 47-50). However, Lin et al fails to render obvious a method of forming a replacement gate stack which includes forming carbon doped sidewall spacers without oxide components and a sacrificial inter-level dielectric layer comprising a stoichiometric silicon nitride. Sugishima et al discloses that it is well known to wet etch silicon oxide with HF. However, Sugishima et al fails to render obvious a method of forming a replacement gate stack which includes forming carbon doped sidewall spacers without oxide components and a sacrificial inter-level dielectric layer comprising a stoichiometric silicon nitride. As such, since Hanafi et al, Lin et al, nor Sugishima et al teach a method of forming a replacement gate stack which includes forming carbon doped sidewall spacers without oxide components and a sacrificial inter-level dielectric layer comprising a stoichiometric silicon nitride the combination of references can not teach or render obvious Applicants' invention as claimed in Claims 1-6 and 8-11.

**PETITION FOR EXTENSION OF TIME**
**PURSUANT TO 37 C.F.R. § 1.136 (a)**

Applicant respectfully petitions pursuant to 37 CFR 1.136(a) for a one-month extension of time to file this response to the Office Action mailed June 27, 2005. The extended period is set to expire on October 27, 2005. A check in the amount of $120.00 is enclosed to cover the fee for a one-month extension of time.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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